Syllabus

General Information

ECE1110 – Computer Organization and Architecture

Instructor: Yong Zhao, 532N

Contact: yong.zhao@scupi.cn

Teaching Assistant: Chaojia Yu

Contact: 2022141520192@stu.scu.edu.cn

Course Meeting Times

Lectures: One session / week, Tuesday 2:00am – 4:35am

Office Hours: Wednesday 2:00pm – 5:00pm and by appointment

Overview

This course is a study of the evolution of computer architecture and the factors influencing the design of hardware and software elements of computer systems. Topics may include: performance, instruction set design; processor micro-architecture and pipelining; cache and virtual memory organizations; protection and sharing; I/O and interrupts; in-order and out-of-order superscalar architectures; vector supercomputers; multithreaded architectures; symmetric multiprocessors; memory models and synchronization; embedded systems; parallel computers; GPU, and cloud computing.

Course Objectives

The goals of the course are to help the students understand the organization and architecture of processors, have basic knowledge of instruction set architectures, and look into details of the design and implementation of the various components that a computer is composed of, and learn the key concepts and approaches to improve the performance and efficiency of modern computers and processors, such as pipelining, caching, virtual memory hierarchy.

Prerequisite

Digital Logic or equivalent

Class Schedule

Lecture slides will be available for copying or posted on BlackBoard.

1. Introduction and review
2. Assembly language
3. Performance
4. Instruction Set
5. MIPS introduction
6. Pipeline
7. Memory hierarchy
8. Cache
9. Virtual memory
10. Security
11. Multiprocessing
12. GPU
13. Large Language Models

Learning Outcome

At the end of the class, the students should be able to understand the following key concepts:

- the organization of a computer system in terms of its components
- the detailed architecture and operation of a microprocessor
- performance measurement and optimization in design and implementation
- the operation of electronic logic elements
- the different characteristics of processor architectures
- MIPS instruction set architecture and basic assembly language programming
- pipeline stages and bypassing/forwarding/branch prediction mechanisms.
- the role and operation of the system memory hierarchy
- caching mechanism
- consistency and synchronization across multiple processors

The students will also have practical experience of basic architectural design and prototyping digital circuits though course projects and relevant tools.

Grades

Grades will be based on homework, course project and final exam.

Homework and attendance: 30%

Course project (1 major project or 2 small projects): 30%

Final Exam: 40%

Collaboration and Academic Honesty Policy

Individual work on all homework and examinations is required, Cheating and copying other students' homework/exam are strictly prohibited. Any violation of this policy will be treated severely.

Collaboration amongst students to understand the course material and to work on course projects is strongly encouraged, however each student should take on different/distinguishable responsibilities in the course projects.

Course Reading Material

Hennessy, J. L., and D. A. Patterson. *Computer Organization and Design: The Hardware/Software Interface*, 6th ed.

This is the main textbook used in this course.

To review the basic material, you may also want to refer:

Patterson, D. A., and J. L. Hennessy. *Computer Architecture: A Quantitative Approach*, 4th ed.

Supplemental readings from selected papers may also be assigned throughout the semester.