❖ 2025F-ECE 0201: Digital Circuits & Systems, Lab

Instructor : Jeungphill Hanne

❖ Agenda for today

1. SCUPI 2025 Fall Academic Calendar

- Academic Calendar : Midterms & Final etc.
- My Schedule : Office hours etc.

2. Course Introduction

- Course information
  - Subject, Text book, Lecture Hour, Office hour, Course website, etc.
- Course Objective & Scope, Course Learning Key Points
- Course Grading & Tentative Course Schedule

3. Call class rolls

4. Brief Introduction of Digital Circuit & Systems

- What is **Digital Circuit & Systems** and Why need **it**
- Scope of **Digital Circuit** and **More**

1. SCUPI 2025 Fall Academic Calendar

- **Academic Calendar : Midterms & Final etc.**

SCUPI Academic Calendar for 2025-2026 Fall

		Sep.				Oct.				Nov.					Dec.				Jan.					Feb.			
Monday	1	8	15	22	29	6	13	20	27	3	10	17	24	1	8	15	22	29	5	12	19	26	2	9	16	23	
Tuesday	2	9	16	23	30	7	14	21	28	4	11	18	25	2	9	16	23	30	6	13	20	27	3	10	17	24	
Wednesday	3	10	17	24	1	8	15	22	29	5	12	19	26	3	10	17	24	31	7	14	21	28	4	11	18	25	
Thursday	4	11	18	25	2	9	16	23	30	6	13	20	27	4	11	18	25	1	8	15	16	29	5	12	19	26	
Friday	5	12	19	26	3	10	17	24	31	7	14	21	28	5	12	19	26	2	9	16	23	30	6	13	20	27	
Saturday	6	13	20	27	4	11	18	25	1	8	15	22	29	6	13	20	27	3	10	17	24	31	7	14	21	28	
Sunday	7	14	21	28	5	12	19	26	2	9	16	23	30	7	14	21	28	4	11	18	25	1	8	15	22	1	
SCU Week	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	
SCU Term	2025 Fall Teaching Weeks																			Final Weeks		Winter Recess					

Notes:
Registration:
Make-up Exams: Sept.4-5
Classes begin: Sept. 08

1st Midterm

2nd Midterm

Final

This schedule is preliminary!!

1. SCUPI 2025 Fall Academic Calendar

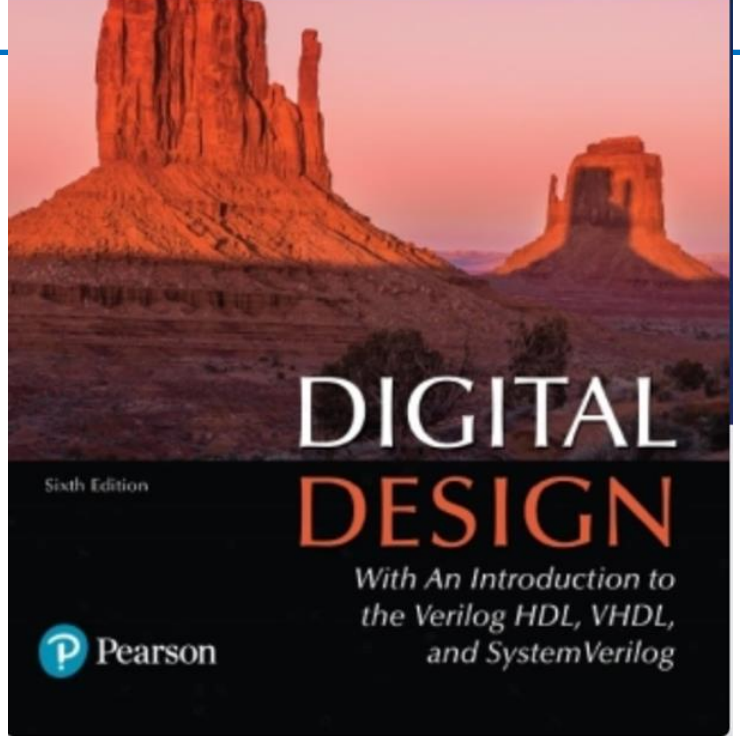
- My Schedule : Office hours etc.

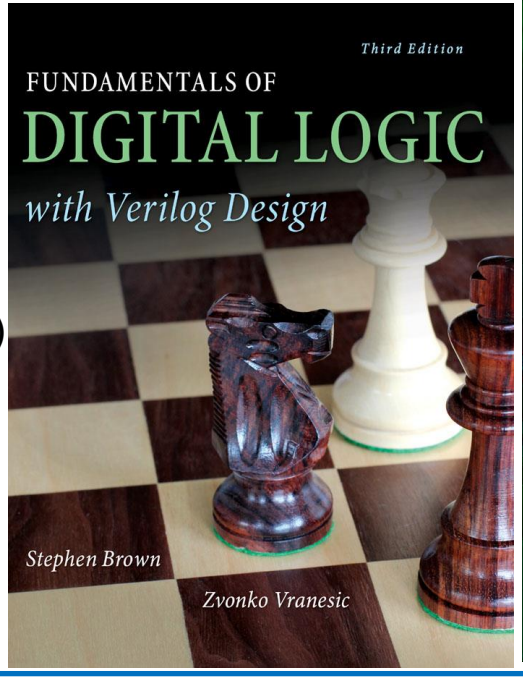
2024-2025 Spring Semester Course Schedule					
Class time	Monday	Tuesday	Wednesday	Thursday	Friday
08:15-09:00					
09:10-09:55					
10:15-11:00	Digital Circuits & Systems ECE 0201 N209 Sec 2		Digital Circuits & Systems ECE 0201 N209 Sec 1		
11:10-11:55	Digital Circuits & Systems ECE 0201 N209 Sec 2		Digital Circuits & Systems ECE 0201 N209 Sec 1		
Lunch Break					
13:50-14:35	Digital Circuits Lab N206/207 Sec 2		Digital Circuits Lab N206/207 Sec 1	Applied Discrete Math Math 0480 S106	
14:45-15:30	Digital Circuits Lab N206/207 Sec 2	Office Hour Sect 1 Digital Circuit N-412	Digital Circuits Lab N206/207 Sec 1	Applied Discrete Math Math 0480 S106	
15:40-16:25	Office Hour Sect 1 Digital Circuit N-412	Office Hour Sect 2 Digital Circuit N-412	Office Hour Sect 2 Digital Circuit N-412	Applied Discrete Math Math 0480 S106	Office Hour Discrete Math N-412
16:45-17:30	Office Hour Sect 2 Digital Circuit N-412	Office Hour Discrete Math N-412	Office Hour Sect 1 Digital Circuit N-412	Office Hour Discrete Math N-412	
17:40-18:25					

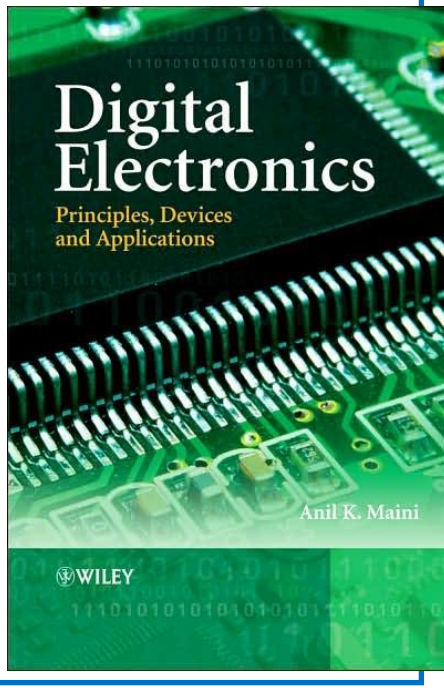
*But, you can come to my office anytime when I am in my office ^^*

2. Course Introduction

- **Digital Circuits & Systems**
  - Learn the fundamentals of ***digital electronics*** and ***computers***. Construct the ***digital*** circuits that perform fundamental computing tasks
- **Text Book:** Digital Design, With an Introduction to the Verilog HDL, VHDL and System Verilog, Mano & Ciletti, 6th ed.,2018, Pearson (ISBN: 9780134549897)
  - **References:** Fundamentals of Digital Logic with Verilog Design, 3rd Ed. S. Brown and Z. Vranesic , 2014 (ISBN 978–0–07–338054–4) McGraw-Hill
  - **:** Digital Electronics, Principles, Devices and Applications A. K. Maini, 2007 (ISBN 978-0-470-03214-5) John Wiley & Sons
- **Lecture** : Jeungphill Hanne, PhD
  jeungphill.hanne@scupi.cn
  - Office Hour: as shown in the Page 3 @ N-412
- **TA**
  - Lecture **:** Rain Ye, Ocean Yu (all ECE juniors)
  - Lab : Aaron Chen, Brian Li (all ECE juniors)
  - Office Hrs : To be announced.
- **Course Format :** Lecture, and Lab
- **Course Grading**
  - Lecture (60~70%) and Lab (30~40%)







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  - **References:** Digital Fundamentals, 11th Ed. Thomas L. Floyd , 2015 Pearson (ISBN: 978-1-292-07598-3)
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- **Lecture** : Jeungphill Hanne, PhD
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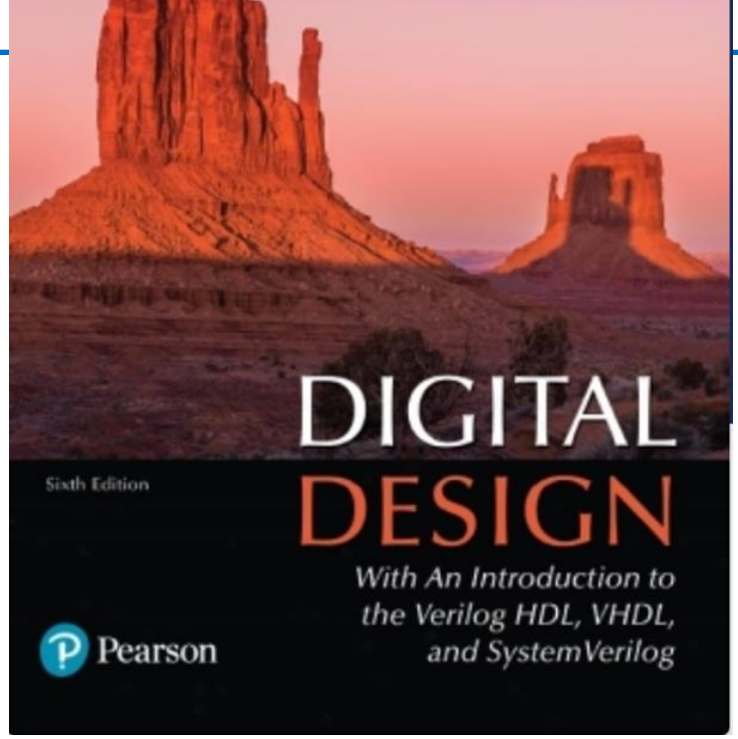
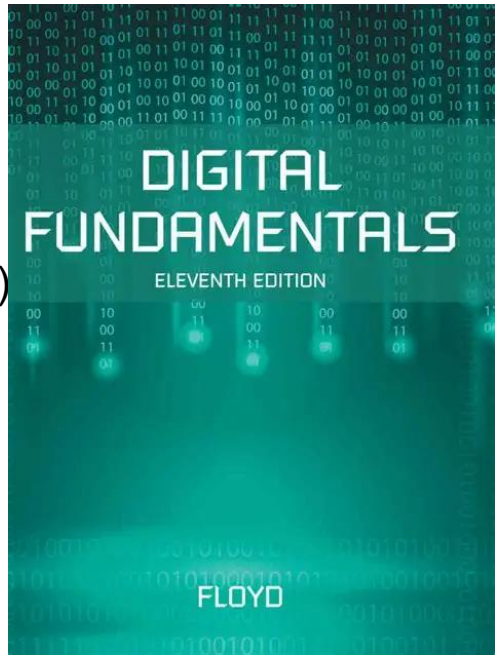
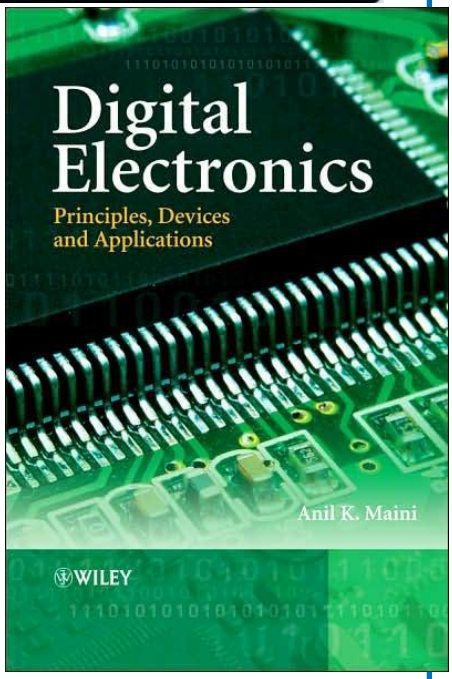






2. Course Introduction

• Course Objective & Scope

- Objective

: Study the fundamental building blocks used in the design of modem ***digital electronics*** and ***computers***. Learn how to use and combine ***digital components*** to create circuits that perform *fundamental computing tasks* such as arithmetic and storage of information.

- Scope & topics

: Primary topics covered include Boolean algebra and binary arithmetic, combinational and sequential logic circuits, Finite-State Machine (FSM), Hardware Design Language (HDL), and Register Transfer Level (RTL) for digital design. Students extend their knowledge to practice by way of hands-on laboratory exercises where various software and hardware tools are used to design and test solutions for real-world applications. After completing this course, students understand the design of digital computing systems at their most fundamental level and are able to craft such systems using modern tools and techniques.

• Course Grading : **Lecture (60~70%) and Lab (30~40%)**

- Lecture Grading : HW(15%), Quiz (5%), Midterm I (24%), Midterm II (24%), Final (25%) and Attitude(5% : Attendance, Focus, Engagement, Punctuality for HW, etc.)

- Lab Grading : Lab Hand Out reports with HW (60%), and Two tests for Labs (Midterm (15%) & Final (15%)), and Attitude (10%, ex. Attendance, Focus, Teamwork, Working Hard, Honesty, etc.)

→ < overall 60% attendance (might be failed for the course!)

• Tentative Course Schedule

Week	ECE_0201(Digital Circuits & Systems)	Topics	Assignment
Week 1 (9/08-9/14)	Introduction & Chap 1	**Syllabus & Introduction on Digital Circuits**	
Week 2 (9/15-9/21)	Chap 1	**Digital Systems and Binary Numbers**	HW1
Week 3 (9/22-9/28)	Chap 2	**Boolean Algebra and Logic Gates**	HW2
Week 4 (9/29-10/05)	Chap 3	**Gate-Level Minimization**	
Week 5 (10/06-10/12)	Chap 3		HW3
Week 6 (10/13-10/19)	Chap 4	**Combinational Logic**	
Week 7 (10/20-10/26)	**Mid Term 1** & Chap 4		HW4
Week 8 (10/27-11/02)	Chap 5	**Synchronous Sequential Logic**	
Week 9 (11/03-11/09)	Chap 5 & Chap 6	**Registers and Counters**	HW5
Week 10 (11/10-11/16)	Chap 6		HW6
Week 11 (11/17-11/23)	Chap 7	**Memory and Programmable Logic**	
Week 12 (11/24-11/30)	Chap 7		HW7
Week 13 (12/01-12/07)	Chap 8 & **Mid Term 2**	**Design at the Register Transfer level**	
Week 14 (12/08-12/14)	Chap 8		HW8
Week 15 (12/15-12/21)	Selected topics	**Finite State Machines (FSM)**	
Week 16 (12/22-12/28)	Selected topics	**FSM Optimizations**	HW9
Week 17 (12/29-01/04)	Selected topics	**Control and Datapath Design**	HW10
Week 18 (01/05-01/11)	Selected topics	**Processor Design**	HW11
Week 19 (01/12-01/18)	Review & **Final**		
Week 20 (01/19-01/25)			

4. Brief Introduction of Digital Circuit & Systems

- What is **Digital Circuit & Systems** and Why need **it** ?
- Scope of **Digital Circuit** and **More**

In the next following pages

4. Brief Introduction of Digital Circuit & Systems

- What is **Digital Circuit & Systems** and Why need **it** ?
- Scope of **Digital Circuit** and **More**

- Two aspects for Digital Circuit & Systems

1) As discretizing the Analog signal and system
→ Digitized Signal and System

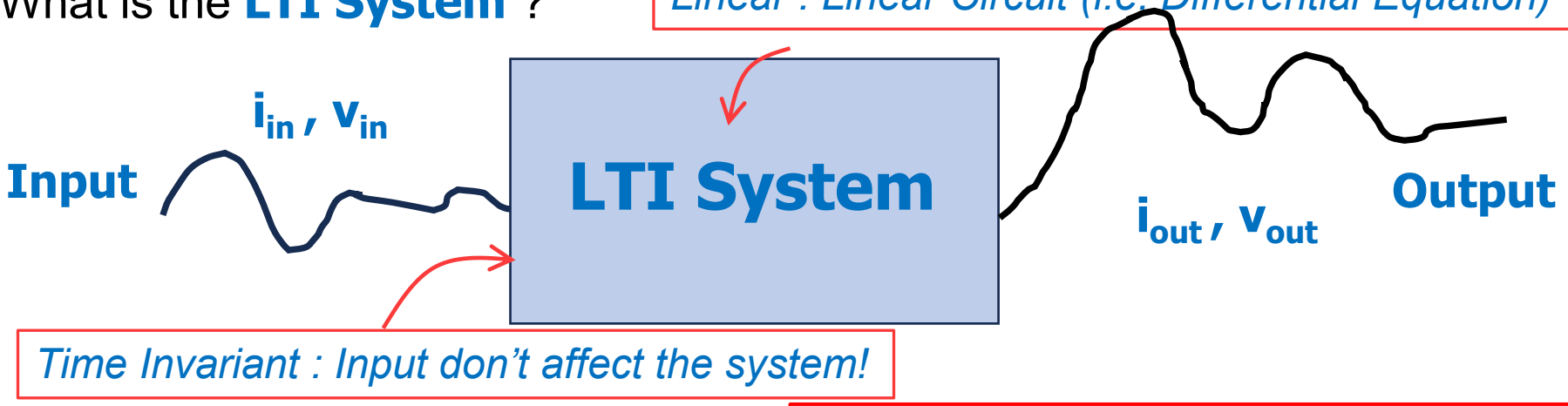
2) As being "computerized" by using the on, or off signal in the electric circuit and more…
→ Our course, mathematically-supported by called "Discrete Mathematics"

1) Digitized Signal and System

- Brief Introduction of the LTI System (Linear-Time-Invariant)

- What is the **LTI System** ?

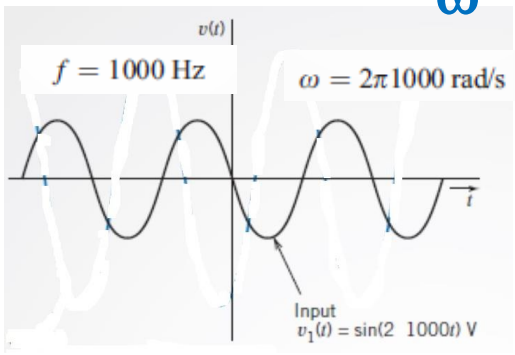
Linear : Linear Circuit (i.e. Differential Equation)

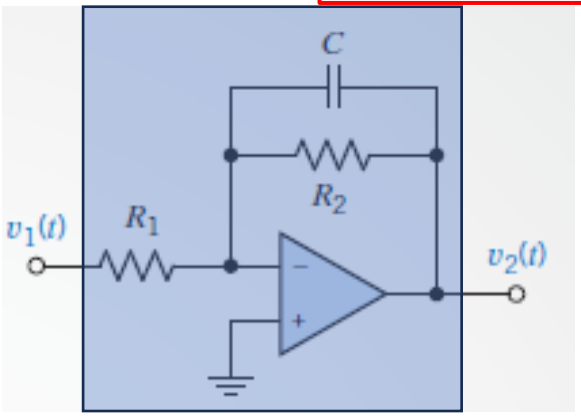


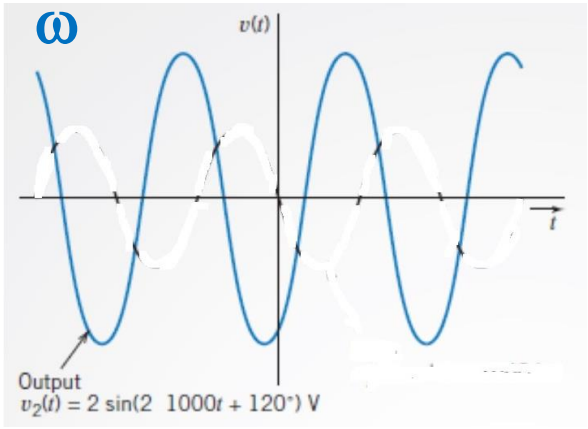
Time Invariant : Input don't affect the system!

- **Example**

H(ω) : Gain, or Transfer function







$v_1(t) = \sin(2\pi 1000t) = \cos(2\pi 1000t - 90^\circ)$ V

<LTI System>

$v_2(t) = 2\sin(2\pi 1000t + 120^\circ) = 2\cos(2\pi 1000t + 30^\circ)$ V

$\mathbf{V}_1 = 1e^{-j90^\circ} = 1\angle -90^\circ$ V **= X(ω)**

$\frac{\mathbf{V}_2}{\mathbf{V}_1} = \frac{2e^{j30^\circ}}{1e^{-j90^\circ}} = 2e^{j120^\circ}$ **=H(ω) =Y(ω)/X (ω)**

$\mathbf{V}_2 = 2e^{j30^\circ}$ V **=Y(ω)= H(ω) X(ω)**

1) Digitized Signal and System

- **Gain & Phase shift → Frequency dependence**

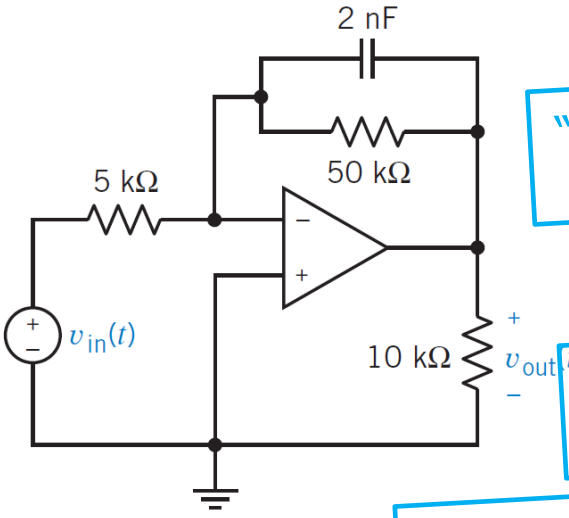


FIGURE 13.2-1 An op amp circuit.

"Steady State Response"
← Forced Response

→Amplitude Changes!
→ Phase Changes!

→But, Frequency don't Changes!

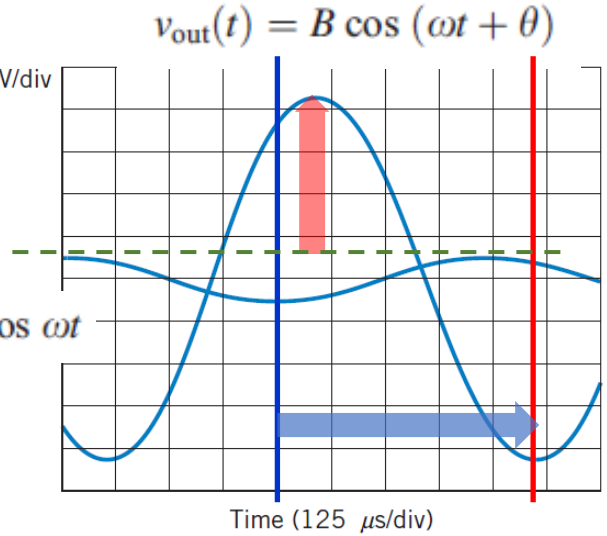


FIGURE 13.2-2 Input and output sinusoids for the op amp circuit of Figure 13.2-1.

"Gain" &"Phase shift"
→ Depends on "Frequency, " f, or ω"

Gain (H)

$$= \frac{\textit{Output Amplitude}}{\textit{Input Amplitude}} = \frac{B}{A}$$

Phase shift

$$= \textit{Output Phase} - \textit{Input Phase}$$

$$= \theta - 0^{\circ}$$

Table 13.2-1 Frequency Response Data for a Circuit

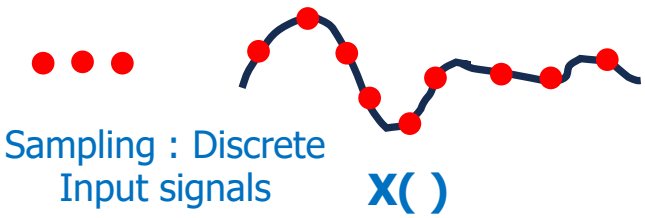
f(Hz)	ω (rad/s)	GAIN	PHASE SHIFT
100	628.3	9.98	176°
500	3,141.6	9.54	163°
1,000	6,283	8.47	148°
5,000	31,416	3.03	108°
10,000	62,830	1.57	99°

1) Digitized Signal and System

- **Electric Filter: Pass one part of the input, but Block the other part of the input (But No original signal change!)**

- Example: Pass "Certain Frequency" but Block "the other Frequency" (But No Amplitude Change!) → Low pass filter by Network Function"

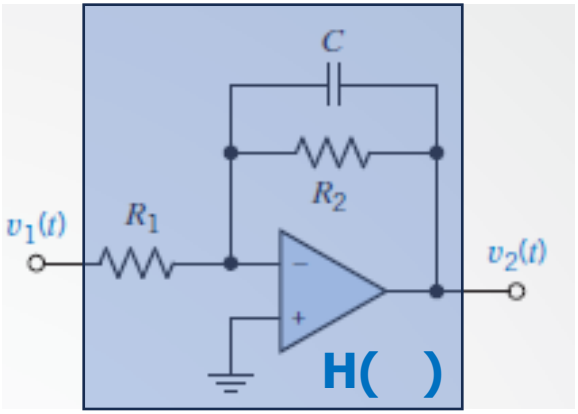
Input i_{in}, V_{in}



Sampling : Discrete Input signals

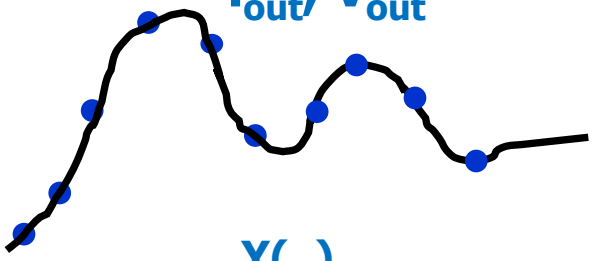
X( )

$\mathcal{F}$ **"Fourier Transform"**



<LTI System>

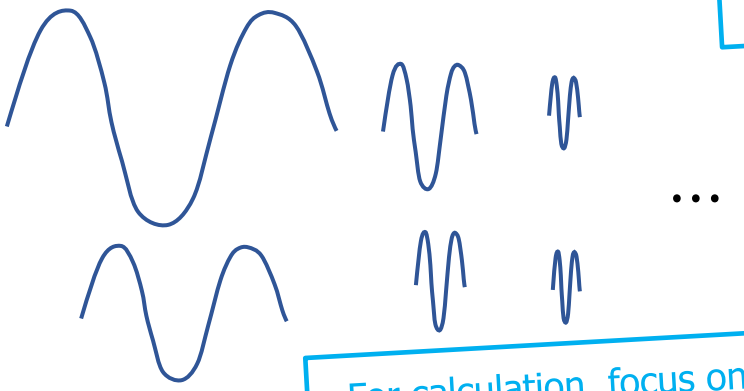
i_{out}, V_{out}



Y( )

Discrete Output signals

← "Low Pass filter" By H(w) "Network" Or "Transfer" function



…

H(ω)

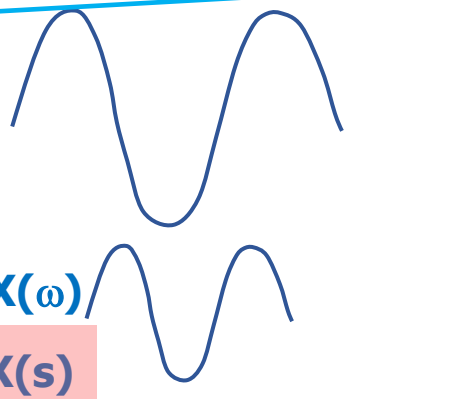
$s = j\omega$

H(s)

$Y(\omega) = H(\omega)\, X(\omega)$

$Y(s) = H(s)\, X(s)$

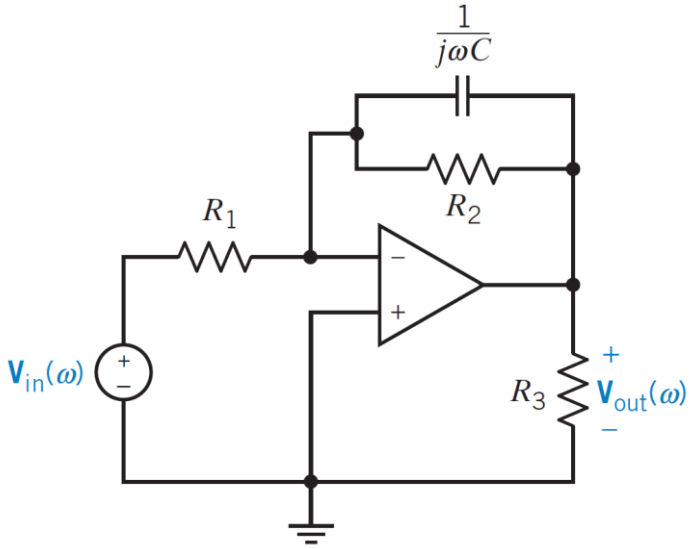
For calculation, focus on "H(s)" →



1) Digitized Signal and System

- **"Low pass filter"**

← Called as **"First Order Low Pass filter"**



$$H(\omega) = \frac{V_{out}(\omega)}{V_{in}(\omega)} = \frac{-R_2}{R_1 + j\omega C R_1 R_2} = \frac{H_0}{1 + j\frac{\omega}{\omega_0}}$$

$$H_0 \equiv -\frac{R_2}{R_1}$$

$$\omega_0 \equiv \frac{1}{\sqrt{R_2 C}}$$

$$\text{gain} = \frac{|H_0|}{\sqrt{1 + \frac{\omega^2}{\omega_0^2}}}$$

When, $\omega \ll \omega_0$ Gain = $|H_0| \rightarrow DC$

Table 13.2-1 Frequency Response Data for a Circuit

f(Hz)	ω (rad/s)	GAIN	PHASE SHIFT
100	628.3	9.98	176°
500	3,141.6	9.54	163°
1,000	6,283	8.47	148°
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10,000	62,830	1.57	99°

$$\text{phase shift} = \angle H_0 - \tan^{-1}(\omega/\omega_0)$$

When $H_0 < 0$, $\angle H_0 = 180^\circ$

& When $H_0 > 0$, $\angle H_0 = 0^\circ$

"Low Frequency "

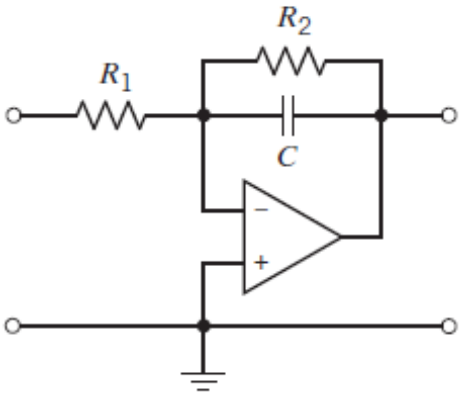
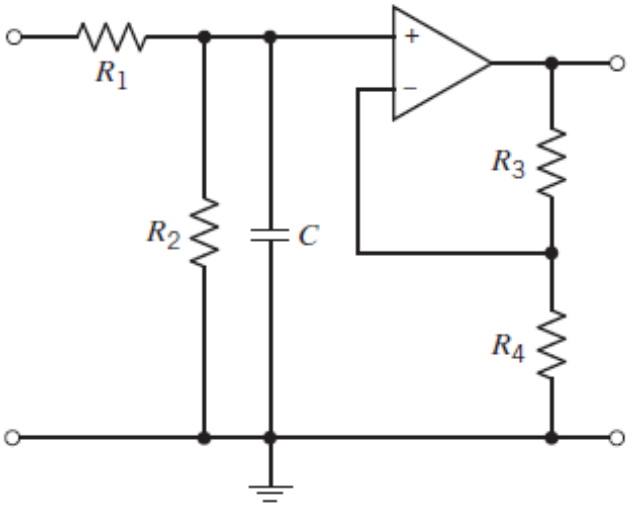
"Gain Decreasing", so Low Frequency Wave signal passes only
→ **"Low Pass filter"**

1) Digitized Signal and System

- **"First-Order Low Pass filter"**

"Low Frequency Wave signal passes only
→ **"Low Pass filter"**

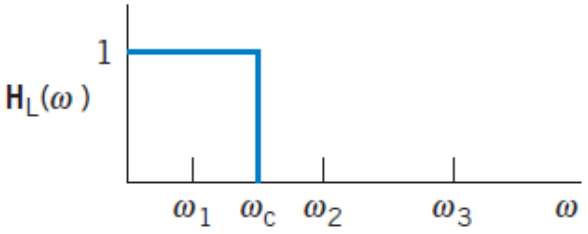
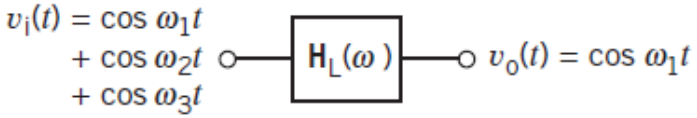
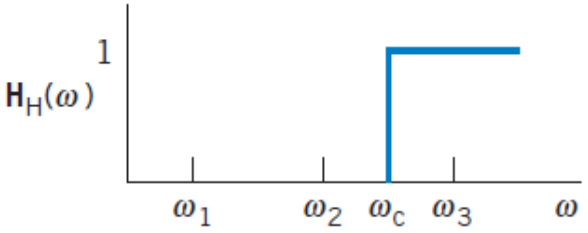
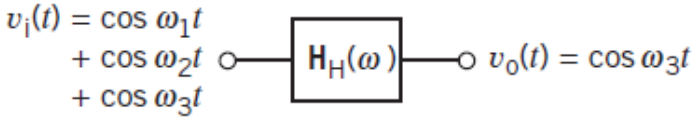
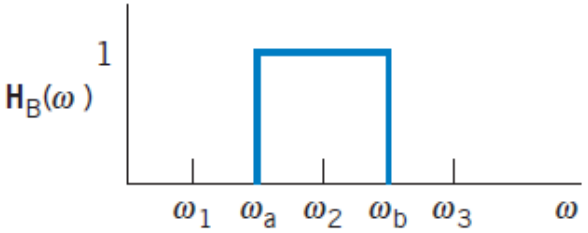
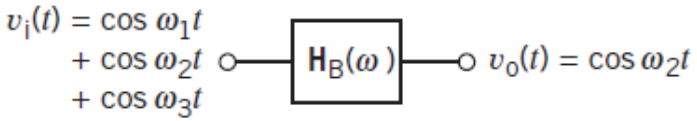
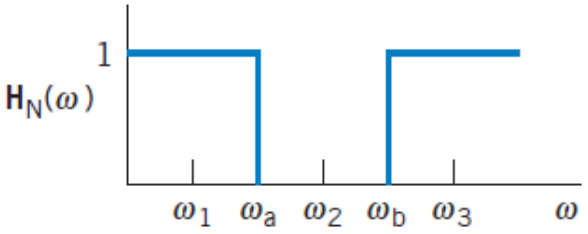
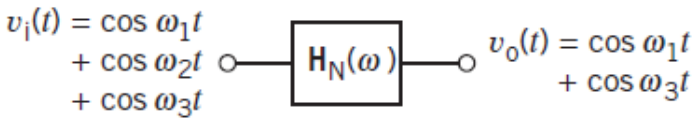
Table 13.2-2 First-Order Low-Pass Filter Circuits

PHASE SHIFT	FIRST-ORDER LOW-PASS FILTER CIRCUIT	DESIGN EQUATIONS
$90° \le \text{phase shift} \le 180°$		$H_0 = -\frac{R_2}{R_1}$ $\omega_0 = \frac{1}{R_2 C}$
$H(\omega) = \frac{H_0}{1 + j\frac{\omega}{\omega_0}}$ $\text{gain} = \frac{\lvert H_0 \rvert}{\sqrt{1 + \frac{\omega^2}{\omega_0^2}}}$ $-90° \le \text{phase shift} \le 0°$		$H_0 = \frac{R_2}{R_1 + R_2}\left(1 + \frac{R_3}{R_4}\right)$ $\omega_0 = \frac{R_1 + R_2}{R_1 R_2 C}$

1) Digitized Signal and System

- **Ideal Filter for "Low Pass", "High Pass", "Band Pass" & "Band Stop(Notch)"**

Table 16.3-1 Ideal Filters

FILTER TYPE	IDEAL FREQUENCY RESPONSE	FILTER INPUT AND OUTPUT
Low-pass		
High-pass		
Band-pass		
Band-stop (notch)		

1) Digitized Signal and System

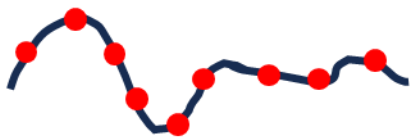
- "Digital Signal & Digital System

- "Why Discrete signals (not continuous signal, " Digital" signal) ?

Continuous Input **Signals**

Input Signal

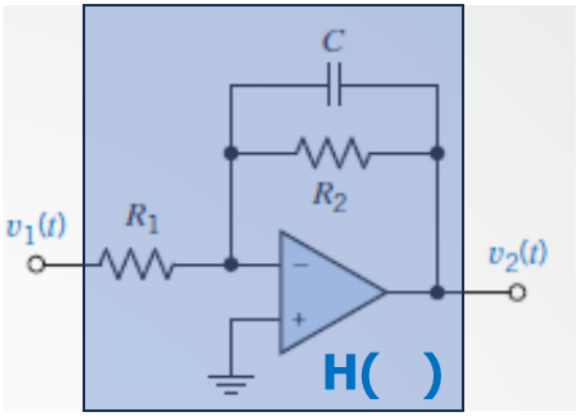
i_{in}, v_{in}



X( )

Sampling : Discrete Input **Signals**

Continuous **System ?**

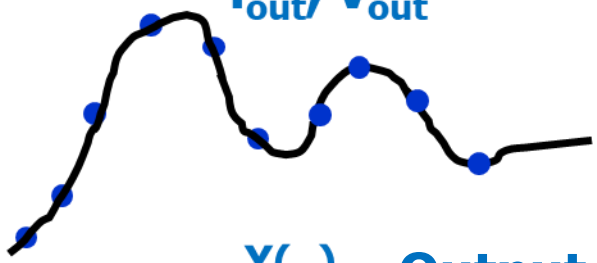


<LTI System>

Linear-Time Invariant

Continuous Output **Signals**

i_{out}, v_{out}



Y( )

Output Signal

Discrete Output **Signals**

- "Analog" signals to "Digital" signal → By ADC (Analog-digital Converter)

- "Digital" signals to "Analog" signal → By DAC (Digital to Analog Converter)

- **How to do it : "Sampling" first → "Converting"**

How to Sample not to lose "information" ?

→ Need to "confirm" it, and how can be done?

How do we know Sampling is good?

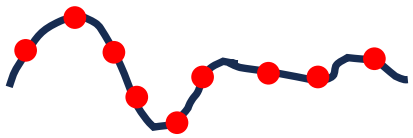
1) Digitized Signal and System

- Analog vs. Digital signal in the LTI System (Linear-Time-Invariant)

H : Gain G, or Transfer function

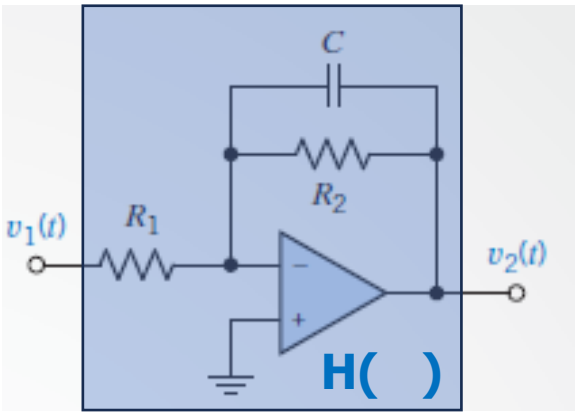
Input Signal

i_{in}, v_{in}



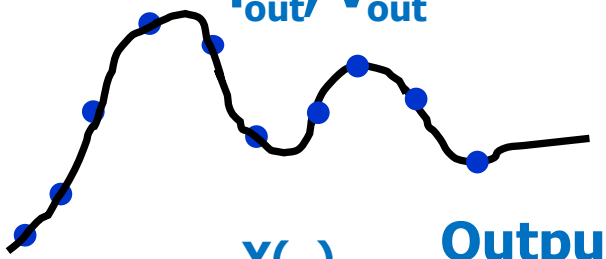
X( )

Sampling : Discrete Input **Signals**



<LTI System>

i_{out}, v_{out}



Y( )

Output Signal

Discrete Output **Signals**

- **Continuous Signal (Analog)**

Fourier Transformation

$X(\omega)$ $H(\omega)$ $Y(\omega)= H(\omega)\, X(\omega)$

Laplace Transformation

$X(s)$ $H(s)$ $Y(s)= H(s)\, X(s)$

- **Discrete Signal(Digital)**

Fourier Series

$X(\omega_n)$ $H(\omega_n)$ $Y(\omega_n)= H(\omega_n)\, X(\omega_n)$

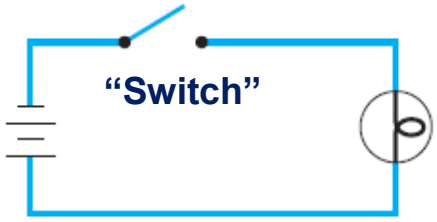
Z Transformation

$X(s_n)$ $H(s_n)$ $Y(s_n)= H(s_n)\, X(s_n)$

2) being "computerized"

- **Digital Logic Circuits** : **Can make the circuits to make realization for "Logic"**

→ **By Switch "On/OFF" in the circuit, "T/F" can be realized, and Circuit "Output"(i.e. current or light bulb on) can detect/represent(?) "Outcome" of "Logics".**

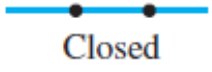


The symbol denotes a battery and the symbol denotes a light bulb.

"Logical statement, p"

"Switch Off"

"F"



"Switch On"

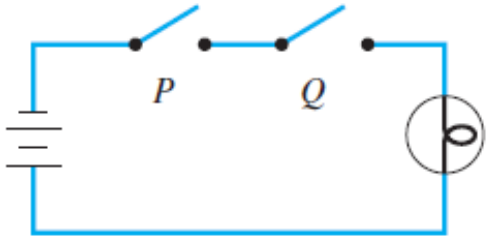
"T"

Truth Table for p

p	
T	"On"
F	"Off"

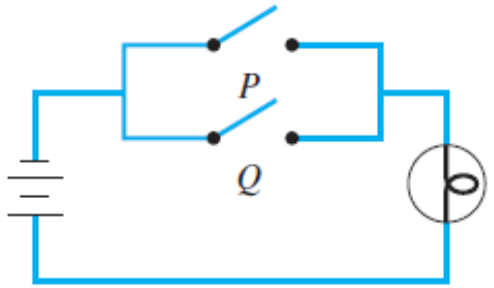
"Circuit/Switch"

- Ex)



Switches "in series"

? What "Logical Table" are matched by them



Switches "in parallel"

Switches		Light Bulb
P	Q	State
closed	closed	on
closed	open	off
open	closed	off
open	open	off

Truth Table for $p \wedge q$

p	q	$p \wedge q$
T	T	T
T	F	F
F	T	F
F	F	F

Switches		Light Bulb
P	Q	State
closed	closed	on
closed	open	on
open	closed	on
open	open	off

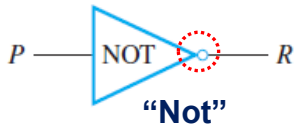
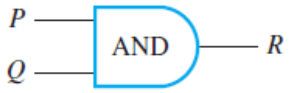
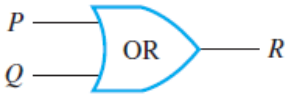
Truth Table for $p \vee q$

p	q	$p \vee q$
T	T	T
T	F	T
F	T	T
F	F	F

2) being "computerized"

• Digital Logic Circuits :Black Boxes and Gates

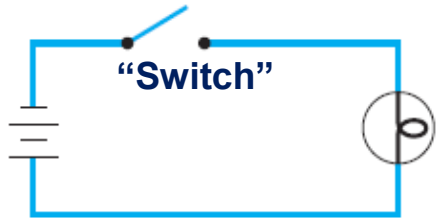
→HW: 2-(6) ? Can we make "Not" by adding something in this(Light bulb) kind of Circuit

Type of Gate	Symbolic Representation	Action
NOT	 "Not"	
AND		
OR		

Input	Output
P	*R*
1	0
0	1

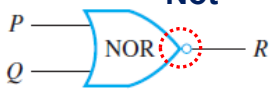
Input		Output
P	*Q*	*R*
1	1	1
1	0	0
0	1	0
0	0	0

Input		Output
P	*Q*	*R*
1	1	1
1	0	1
0	1	1
0	0	0



So.. → "Not"

"Logical statement, p" "~p"

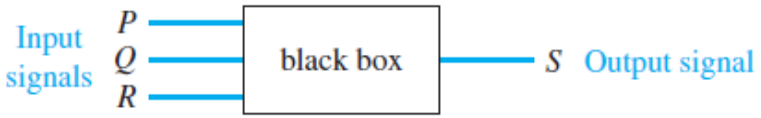
Type of Gate	Symbolic Representation	Action
NAND	 "Not"	
NOR	"Not"  "Exclusive or?"	

Input		Output
P	*Q*	$R = P \mid Q$
1	1	0
1	0	1
0	1	1
0	0	1

Input		Output
P	*Q*	$R = P \downarrow Q$
1	1	0
1	0	0
0	1	0
0	0	1

2) being "computerized"

• Digital Logic Circuits : The Input/Output Table for a Circuit

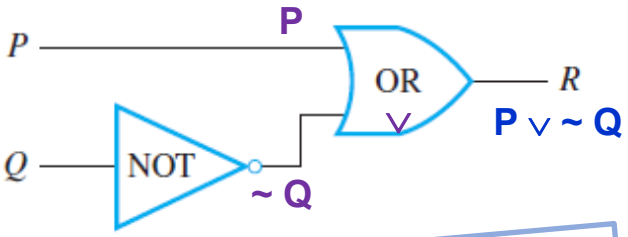


→HW: 2-(7)
? What is the circuit to produce this "Truth table'?

Input			Output
P	Q	R	S
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	1
0	1	1	0
0	1	0	1
0	0	1	1
0	0	0	0

Example 2.4.2 Constructing the Input/Output Table for a Circuit

Construct the input/output table for the following circuit.



? What "Logical Expression (Boolean expression)" for it?

P ∨ ~ Q

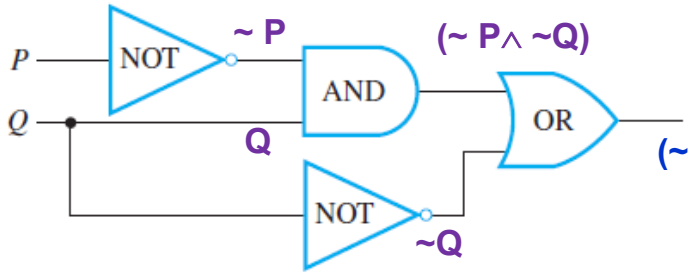
Input		Output
P	Q	R
1	1	1
1	0	1
0	1	0
0	0	1

P ∨ ~ Q : *Boolean expression*

Example 2.4.4 Constructing Circuits for Boolean Expressions

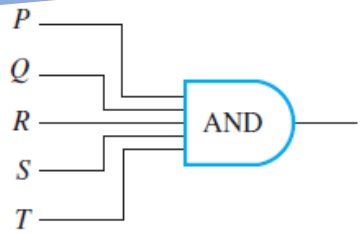
Construct circuits for the following Boolean expressions.

a. $(\sim P \wedge Q) \vee \sim Q$



b. $((P \wedge Q) \wedge (R \wedge S)) \wedge T$

→ *How about this one?, Can be more clear and simplified? How?*



2) being “computerized”

- **Digital Logic Circuits : Boolean Expression & Electrical Circuit (“Design”)**

Example 2.4.5 Designing a Circuit for a Given Input/Output Table

Design a circuit for the following input/output table:

Input			Output
P	*Q*	*R*	*S*
1	1	1	1
1	1	0	0
1	0	1	1
1	0	0	1
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	0

$P \wedge Q \wedge R$

$\vee$

$P \wedge \sim Q \wedge R$

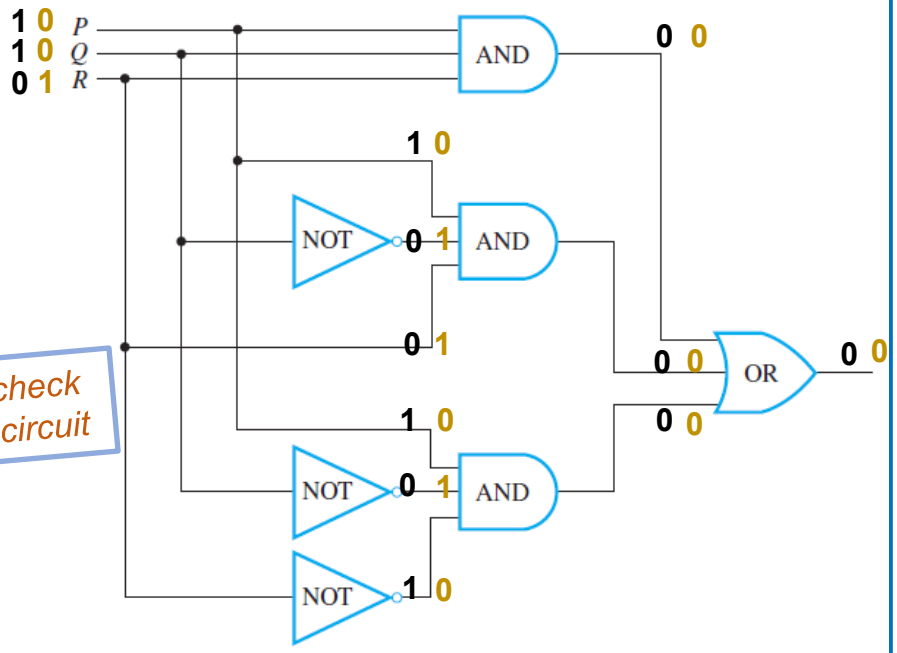
$\vee$

$\sim P \wedge \sim Q \wedge \sim R$

Let’s check in the circuit

$(P \wedge Q \wedge R) \vee (P \wedge \sim Q \wedge R) \vee (\sim P \wedge \sim Q \wedge \sim R)$

- **Some possible tips**
1. First consider the possible “and” circuits, by focusing on “T” outputs
2. Connect them by “or”
3. And check…



- **NAND & NOR**

Example 2.4.7 Rewriting Expressions Using the Sheffer Stroke

Use Theorem 2.1.1 and the definition of Sheffer stroke to show that

a. $\sim P \equiv P \mid P$ and b. $P \vee Q \equiv (P \mid P) \mid (Q \mid Q)$.

2) being "computerized"

• Binary Number Systems and Circuits for Addition

① Binary Representation of Numbers

• **Number in Decimal (form) : Express the number by "Decimal" (0,1,2,…,9)**
→ **Having k_{th} digit in Decimal form**

$$0 \le a_n \le 9$$
$$a_k a_{k-1} \cdots a_1 a_0 = \sum_{n=0}^{k} a_n 10^n$$

$$5{,}049 = 5\cdot(1{,}000) + 0\cdot(100) + 4\cdot(10) + 9\cdot(1) = 5\cdot 10^3 + 0\cdot 10^2 + 4\cdot 10^1 + 9\cdot 10^0$$

$$= 5{,}049_{10}$$

Place	10^3 thousands	10^2 hundreds	10^1 tens	10^0 ones
Decimal Digit	5	0	4	9

• **Number in Binary (form) : Express the number by "Binary" (0,1)**
→ **Having k_{th} digit in Binary form**

$$0 \le b_n \le 1$$
$$b_k b_{k-1} \cdots b_1 b_0 = \sum_{n=0}^{k} b_n 2^n$$

$$11011_2 = 1\cdot 2^4 + 1\cdot 2^3 + 0\cdot 2^2 + 1\cdot 2^1 + 1\cdot 2^0$$

Place	2^4 sixteens	2^3 eights	2^2 fours	2^1 twos	2^0 ones
Binary Digit	1	1	0	1	1

$$= 16 + 8 + 2 + 1 = 27 = 27_{10}$$

→ *This is how two expressions are related to each other*

$$\begin{aligned}
1_{10} &= 1\cdot 2^0 = 1_2 \\
2_{10} &= 1\cdot 2^1 + 0\cdot 2^0 = 10_2 \\
3_{10} &= 1\cdot 2^1 + 1\cdot 2^0 = 11_2 \\
4_{10} &= 1\cdot 2^2 + 0\cdot 2^1 + 0\cdot 2^0 = 100_2 \\
5_{10} &= 1\cdot 2^2 + 0\cdot 2^1 + 1\cdot 2^0 = 101_2 \\
6_{10} &= 1\cdot 2^2 + 1\cdot 2^1 + 0\cdot 2^0 = 110_2 \\
7_{10} &= 1\cdot 2^2 + 1\cdot 2^1 + 1\cdot 2^0 = 111_2 \\
8_{10} &= 1\cdot 2^3 + 0\cdot 2^2 + 0\cdot 2^1 + 0\cdot 2^0 = 1000_2 \\
9_{10} &= 1\cdot 2^3 + 0\cdot 2^2 + 0\cdot 2^1 + 1\cdot 2^0 = 1001_2
\end{aligned}$$

Power of 2	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Decimal Form	1024	512	256	128	64	32	16	8	4	2	1

2) being "computerized"

• Binary Number Systems and Circuits for Addition

① Binary Representation of Numbers

Example 2.5.2 Converting a Binary to a Decimal Number

Represent 110101_2 in decimal notation

$$0 \le b_n \le 1$$
$$b_k b_{k-1} \cdots b_1 b_0 = \sum_{n=0}^{k} b_n 2^n$$

Example 2.5.3 Converting a Decimal to a Binary Number

Represent 209 in binary notation.

$$0 \le a_n \le 9$$
$$a_k a_{k-1} \cdots a_1 a_0 = \sum_{n=0}^{k} a_n 10^n$$

② Binary Addition and Subtraction

Example 2.5.4 Addition in Binary Notation

Add 1101_2 and 111_2 using binary notation.

$$\begin{array}{rcccc} & 1 & 1 & 1 & \leftarrow \text{carry row} \\ & 1 & 1 & 0 & 1_2 \\ + & & 1 & 1 & 1_2 \\ \hline 1 & 0 & 1 & 0 & 0_2 \end{array}$$

Example 2.5.5 Subtraction in Binary Notation

Subtract 1011_2 from 11000_2 using binary notation.

$$\begin{array}{rcccc} & 0 & 1 & 1 & \\ & \not{1} & \not{1} & 1 & \leftarrow \text{borrow row} \\ 1 & \not{1} & \not{0} & 0 & 0_2 \\ - & 1 & 0 & 1 & 1_2 \\ \hline & 1 & 1 & 0 & 1_2 \end{array}$$

2) being "computerized"

• Binary Number Systems and Circuits for Addition

③ Circuits for Computer Addition

→ Circuit for "Binary addition"

• Addition of "Two Binary 1st digits, P(0,1), Q(0,1)" : Half-Adder

"Carry"

P Q

$1_2 + 1_2 = 10_2$

$1_2 + 0_2 = 1_2 = 01_2$

$0_2 + 1_2 = 1_2 = 01_2$

$0_2 + 0_2 = 0_2 = 00_2$

"Sum"

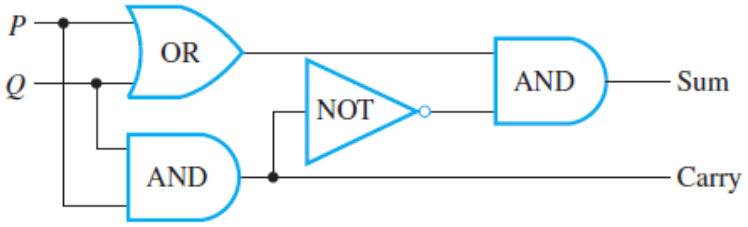
"Exclusive Or"

P	Q	Carry	Sum
1	1	1	0
1	0	0	1
0	1	0	1
0	0	0	0

"And"

- Ex)

$$\begin{array}{r} P \quad (0,1) \\ +\ Q \quad (0,1) \\ \hline CS \end{array} \qquad \begin{array}{r} 1_2 \\ 1_2 \\ \hline 10_2 \end{array}$$



<Half-Adder circuit>

• Addition of "Three 1st digits, P (0,1), Q(0,1), R(0,1)" : Full-Adder

- When adding "two binary numbers", need to add "Three 1st digits" together

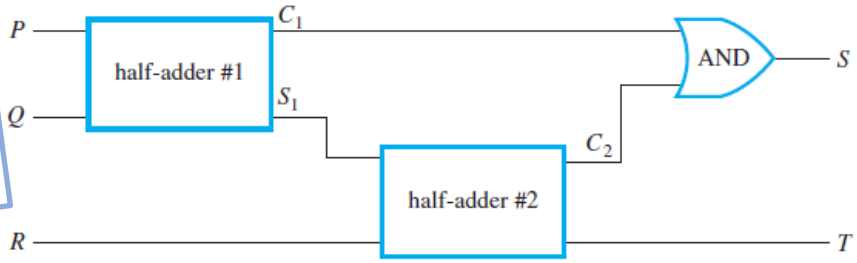
$$\begin{array}{r} 1\ 1\ 1_2 \\ +\ 1\ 1\ 1_2 \\ \hline 1\ 1\ 0_2 \end{array}$$

"Half-Adder"

"Full-Adder"

$$\begin{array}{r} P \\ +\ Q \\ \hline C_1 S_1 \end{array} \qquad \begin{array}{r} C_1 S_1 \\ +\ R \\ \hline C_2 S \end{array} \qquad \begin{array}{r} P \\ +\ Q \\ +\ R \\ \hline CS \end{array} \qquad \begin{array}{r} S_1 \\ +\ R \\ \hline C_2 S \end{array}$$

→ ? Is it possible for C1=1 & C2=1 at the same time



<Full-Adder circuit>

• 2–5 Application: Number Systems and Circuits for Addition

3) Circuits for Computer Addition

→ Circuit for "Binary addition"

• Addition of "Two Three-digit Binary Numbers PQR+STU=WXYZ, where P's is (0,1). : **Parallel-Adder**

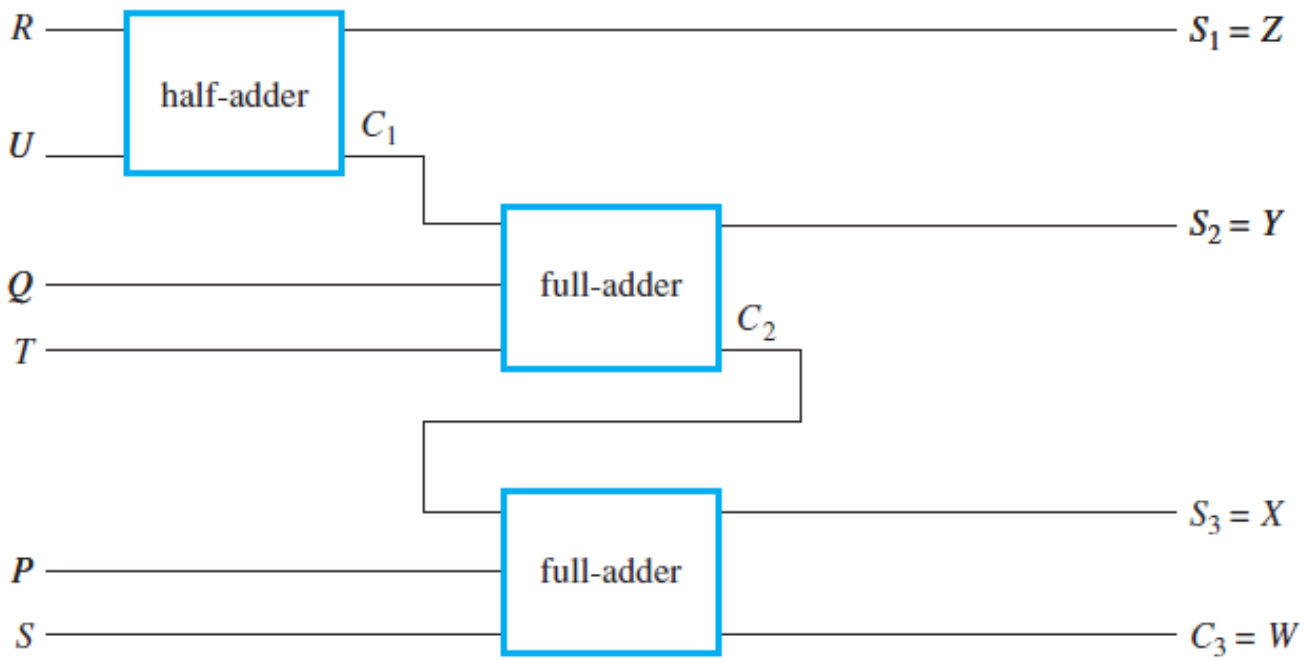


Figure 2.5.3 A Parallel Adder to Add PQR and STU to Obtain $WXYZ$

→HW: 2-(8) : please show this works!

Thank you everybody!

, And See you next time for Chap 1

Digital Systems and Binary Numbers

3. ECE_0201(Digital Circuits & System)_Lab Course

Instructor : Jeungphill Hanne
Lab Coordinator : Aaron Chen (sect 1) & Brian Li (sect 2)

- **Text Book**
  - Lab Hand outs for each lab (will be download in BB)
- **Lab Coordinator**
  - Aaron Chen, Junior student at SCUPI ECE
    2023141520295@stu.scu.edu.cn : Office Hour/Office will be announced
  - Brian Li, Junior student at SCUPI ECE
    2023141520010@stu.scu.edu.cn : Office Hour/Office will be announced
- **Lab Course Format**
  - Perform Lab (2 hour per week) with a group members and Submit Lab report with HW from Hand out
  - The total 12 labs will be executed almost every week, and two tests for labs will be offered.
- **Course Grading (Lab will cover the 30~40% of the ECE_0201 grade)**
  (Thus, the course lecture will cover the 60~70% of the ECE_0201 grade)
  - **Lab grading :**
    Lab Hand out reports with HW (60%), and Two tests for Labs (Midterm (15%) & Final (15%)), and Attitude (10%, ex. Attendance, Focus, Teamwork, Working Hard, Honesty, etc.)

Can be Flexible!

• Tentative Lab Course Schedule

Week	ECE 0201 (Digital Circuits & Systems)	Topics	Assignment
Week 1 (9/08-9/14)	Introduction	**Introduction , Group Sorting & Lab Safety**	
Week 2 (9/15-9/21)	Lab 1	**Logic Abstraction (Breadboard, Switches)**	HW
Week 3 (9/22-9/28)	Lab 2	**Transistors as Switches (Breadboard, Discrete Transistors)**	HW
Week 4 (9/29-10/05)	Lab 3	**Digital Logic Gates (7400-Series)**	HW
Week 5 (10/06-10/12)	Break		
Week 6 (10/13-10/19)	Lab 4	**Simplification of Boolean Functions (7400-Series)**	HW
Week 7 (10/20-10/26)	Lab 5	**Combinational Circuits (7400-Series)**	HW
Week 8 (10/27-11/02)	Lab 6	**Introduction to Field Programmable Gate Arrays (FPGA)**	HW
Week 9 (11/03-11/09)	Break		
Week 10 (11/10-11/16)	**Mid Term**	**Range : Lab1-Lab6**	
Week 11 (11/17-11/23)	Lab 7	**Logic Design with Combinational Logic Building Blocks (FPGA}**	HW
Week 12 (11/24-11/30)	Lab 8	**Latches, Flip-Flops and Registers (FPGA)**	HW
Week 13 (12/01-12/07)	Lab 9	**Arithmetic Circuit Implementations (FPGA)**	HW
Week 14 (12/08-12/14)	Break		
Week 15 (12/15-12/21)	Lab 10	**Counters (FPGA)**	HW
Week 16 (12/22-12/28)	Lab 11	**Finite State Machines (FPGA)**	HW
Week 17 (12/29-01/04)	Lab 12	**Design of a simple CPU (FPGA)**	HW
Week 18 (01/05-01/11)	Break		
Week 19 (01/12-01/18)	**Final**	**Range : Lab7-Lab12**	
Week 20 (01/19-01/25)			

❖ Handling the data from the measurements

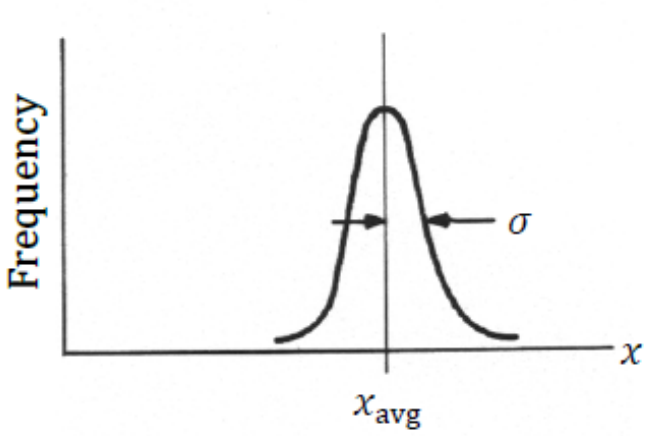
1. Significant Digits

Examples
The period of a pendulum is given by $T = 2\pi\sqrt{l/g}$. Here, $l = 0.24\text{m}$ is the pendulum length and $g = 9.81\text{m/s}^2$ is the acceleration due to gravity. ✗ **WRONG:** $T = 0.983269235922\text{s}$ ✓ **RIGHT:** $T = 0.98\text{s}$ Your calculator may report the first number, but there is no way you know T to that level of precision. When no uncertainties are given, report your value with the same number of significant figures as the value with the smallest number of significant figures.
The mass of an object was found to be 3.56g with an uncertainty of 0.032g. ✗ **WRONG:** $m = 3.56 \pm 0.032\text{g}$ ✓ **RIGHT:** $m = 3.56 \pm 0.03\text{g}$ The first way is wrong because the uncertainty should be reported with one significant figure
The length of an object was found to be 2.593cm with an uncertainty of 0.03cm. ✗ **WRONG:** $L = 2.593 \pm 0.03\text{cm}$ ✓ **RIGHT:** $L = 2.59 \pm 0.03\text{cm}$ The first way is wrong because it is impossible for the third decimal point to be meaningful since it is smaller than the uncertainty.

2. Average and Standard deviation (i.e. Measure at least 5 times and more)

If only random errors affect a measurement, it can be shown mathematically that in the limit of an **infinite** number of measurements ($N \to \infty$), the distribution of values follows a **normal distribution** (i.e. the bell curve on the right). This distribution has a peak at the mean value x_{avg} and a width given by the standard deviation σ.

Obviously, we never take an infinite number of measurements. However, for a large number of measurements, say, $N \sim 10^2$ or more, measurements may be approximately normally distributed. In that event we use the formulae below:



Mean (x_{avg})	The average of all values of x (the "best" value of x). This is the same as for small data sets.	$x_{avg} = \frac{\sum_{i=1}^{N} x_i}{N}$
Uncertainty in a measurement (Δx)	Uncertainty in a single measurement of x. The vast majority of your data lies in the range $x_{avg} \pm \sigma$	$\Delta x = \sigma = \sqrt{\frac{\sum_{i=1}^{N}(x_i - x_{avg})^2}{N}}$
Uncertainty in the Mean (Δx_{avg})	Uncertainty in the mean value of x. The actual value of x will be somewhere in a neighborhood around x_{avg}. This neighborhood of values is the uncertainty in the mean.	$\Delta x_{avg} = \frac{\sigma}{\sqrt{N}}$
Measured Value (x_m)	The final reported value of a measurement of x contains both the average value and the uncertainty in the mean.	$x_m = x_{avg} \pm \Delta x_{avg}$

3. Error propagation

1. If x and y have independent random errors δx and δy, then the error in $z = x + y$ is

$$\delta z = \sqrt{\delta x^2 + \delta y^2}.$$

2. If x and y have independent random errors δx and δy, then the error in $z = x \times y$ is

$$\frac{\delta z}{z} = \sqrt{\left(\frac{\delta x}{x}\right)^2 + \left(\frac{\delta y}{y}\right)^2}.$$

3. If $z = f(x)$ for some function $f()$, then

$$\delta z = |f'(x)|\delta x.$$

3. Error propagation

Ex).

Problem: To find the volume of a certain cube, you measure its side as $2.00 \pm 0.02\,\text{cm}$. Convert this uncertainty to a percent and then find the volume with its uncertainty.

Solution: The volume V is given in terms of the side s by

$$V = s^3,$$

so the uncertainty in the volume is, by rule 3,

$$\delta V = 3s^2\,\delta s = 0.24,$$

and the volume is $8.0 \pm 0.2\,\text{cm}^3$.

General Formula for Error Propagation

We measure $x_1, x_2 \ldots x_n$ with uncertainties $\delta x_1, \delta x_2 \ldots \delta x_n$. The purpose of these measurements is to determine q, which is a function of $x_1, \ldots, x_n$:

$$q = f(x_1, \ldots, x_n).$$

The uncertainty in q is then

$$\delta q = \sqrt{\left(\frac{\partial q}{\partial x_1}\delta x_1\right)^2 + \ldots + \left(\frac{\partial q}{\partial x_n}\delta x_n\right)^2}$$

Thank you everybody!

, And See you next time for Lab 1