Sichuan University - Pittsburgh Institute

ECE 0201 **Digital Circuits and Systems** **Fall 2024**

Note: This syllabus is subject to changes during the semester. Any changes to the syllabus will be announced in class or posted on the Blackboard course area.

Description: In this course, students will learn about fundamental components and techniques used in the design of digital electronics and computers. Topics covered include: Boolean algebra and binary arithmetic, combinational and sequential logic circuits, Finite State Machines (FSMs), Hardware Design Language (HDL), and Register Transfer Level (RTL) for digital design. Students will apply knowledge of these topics in hands-on laboratory exercises to practice designing and testing solutions for real-world applications using modern tools and techniques.

Instructor: Dr. Fashu Xu
Office Hours: Monday, or by appointment
Location: Rm 103, 2nd Teaching Building, East District, Huaxi Campus
Email: xufs@scu.edu.cn **(Please include "ECE 0201" and some topic keywords in the subject line.)**

Teaching Assistants:
Wenwen Yang (for Lectures)
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Lectures: Mon. 8:15 – 9:55 AM, Zone 3 - 106
Labs: Mon. 1:50 – 3:30 PM (Session 1), New Building 206
4:45 – 6:25 PM (Session 2), New Building 206

Textbook: *Digital Design: With an Introduction to the Verilog HDL, VHDL and System Verilog, Mano & Ciletti, 6th Edition, Pearson*

Grading:

Homework	10%
Quizzes	5%
Labs	40%
Midterm Exam I	15%

Midterm Exam II 15%
Final Exam 15%

Letter grades will be determined from accumulated point totals and assigned according to the scale below.

A: 90 - 100	A-: 85 - 90	B+: 80 - 85	B: 76 - 80	B-: 73 - 76
C+: 70 - 73	C: 66 - 70	C-: 63 - 66	D: 60 - 63	F: < 60

Note: Up to 5% points could be granted to the final grade based on the overall course performance (lecture and lab attendance, assignment (homework and lab reports) submission punctuality, course engagement such as in-class question answering and discussion, etc.).

Homework: Homework problems will be assigned throughout the semester. All finished homework needs to be submitted online by the specified due date. Homework will be graded and solutions for all homework problems will be posted 48 hours after the submission due date. The lowest one homework grade will be dropped when calculating final grades. While discussion between students is allowed for solving homework problems, each student must write and submit the homework individually.

Quizzes: In-class quizzes will be arranged generally prior to the exams. Each quiz will have up to a few questions or problems related to the learned content and help the preparation for exams. The lowest one quiz grade will be dropped when calculating final grades. Each student must complete the quizzes individually.

Exams: There will be two midterm exams and one final exam. See the schedule below and any updates on Blackboard.

Labs: This course has an accompanying laboratory component. Students are required to complete pre-lab assignments associated with each lab and submit a lab report the week following the finishing of each lab topic. Students will be working as groups to do experiments and write lab reports, and members of the same group will receive the same grade if no one gets deduction of points due to poor lab performance judged by the instructor. Lab instructions will be posted and lab reports will be submitted both online on Blackboard.

Late Work and Make-up Policy: Late assignment (homework and lab reports) submission will be accepted up to 48 hours after the initial due date with a 20% penalty, unless an extension request is approved **prior to the assignment due date**. Extensions are granted at the instructor's discretion. In general, **no** make-ups for quizzes and exams will be allowed. Exceptions will only be made for special circumstances such as a medical emergency. If you cannot attend a quiz or an exam, you must contact the instructor prior to the quiz and exam. Failure to do so will result in a zero grade on that quiz or exam.

Grade Rebuttal: For any quiz or exam, you have one week to request correction if you feel your answer might be mis-graded. No correction will be made a week after the quiz or exam grade is posted.

Disability Services: If you have a disability for which you are or may be requesting an accommodation, you are encouraged to contact the instructor as early as possible in the semester. Reasonable accommodations will be arranged for this course.

Communication with Instructor for Absence: In any situation regarding class (lectures or labs) absence, a student who becomes ill or has other emergency issues is responsible for communicating with the instructor. Please contact the instructor via email as soon as possible prior to the class to be involved.

Academic Integrity: Students in this course will be expected to comply with the SCUPI and/or University of Pittsburgh's Policy on Academic Integrity. Any student suspected of violating this obligation for any reason during the semester will be required to participate in the procedural process, initiated at the instructor level, as outlined in the University Guidelines on Academic Integrity. This may include, but is not limited to, the confiscation of the examination of any individual suspected of violating University Policy.

Audio/Video Recording: To ensure free and open discussion, students may not record lectures, labs, discussions and/or any other class activities without the advance written permission from the instructor, and any such recording properly approved in advance can solely be limited to the student's own private use.

Lecture Schedule: The table below lists topics that will be covered (subject to changes).

Part 1: Binary Numbers, Boolean Algebra, Logic Circuits and Gate-Level Minimization
Introduction, Binary Logic
Binary Numbers, Number-Base Conversions, Octal and Hex Numbers
Axioms, Theorems, and Properties of Boolean Algebra
Boolean Algebra, Canonical Forms, Logic Gates
Implementation Technologies, CMOS
Gate-Level Minimization with K-Maps
Algorithms for Logic Minimization, IC Digital Logic Gates
Multi-Level Circuits, NAND/NOR and XOR Implementations
Design of Combinational Circuits
Exam 1
Part 2: Combinational Logic Components, Binary Arithmetic, HDLs, Latches and Flip- Flops

Hardware Description Languages, Simulation
Multiplexers, Encoders, Decoders
Multiplexer and Decoder Synthesis
Binary Adders
Carry-Lookahead Adders, Signed Number Representation
Sequential Circuits, Latches, Flip-Flops
Analysis of Circuits Containing Flip-Flops
Registers and Counters
Exam 2
Part 3: FSM, Memory, Programmable Logic, RTL Design, ASM
Design of Flip-Flop Circuits
Mealy and Moore Finite State Machines
FSM Design and Optimization
Random-Access Memory, Memory Decoding, Programmable Logic
RTL Descriptions, Algorithmic State Machines (ASMs)
Processor Design
Final Exam

Lab Schedule (Subject to Changes)

Lab	Topic	Equipment Focus
1	Logic Abstraction	Breadboard, Switches
2	Transistors as Switches	Breadboard, Discrete Transistors
3	Integrated Circuit Digital Logic Gates	7400-Series Chips
4	Design of Combinational Logic Circuits	7400-Series Chips
5	Optimized Implementations of Logic Functions	7400-Series Chips
6	Introduction to Field Programmable Gate Arrays	FPGA
7	Combinational Logic Building Blocks	FPGA
8	Adders and Arithmetic Circuits	FPGA
9	Latches and Flip Flops	FPGA
10	Counters and Sequential Circuits	FPGA
11	Finite State Machines	FPGA